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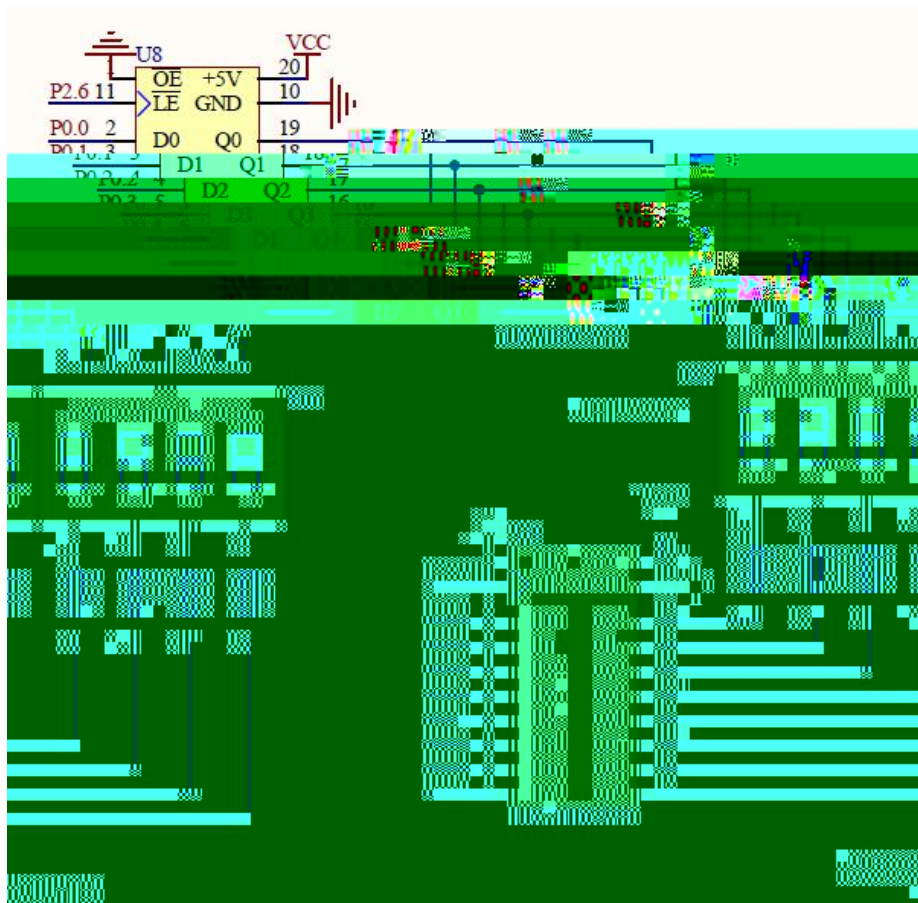








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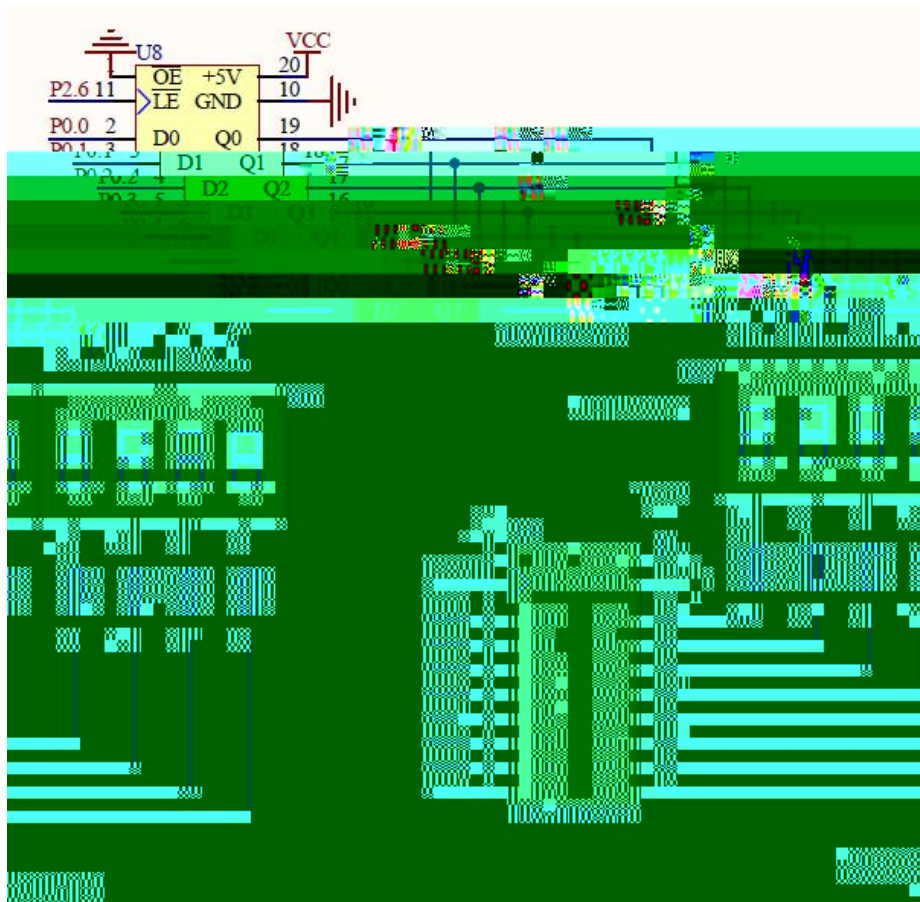
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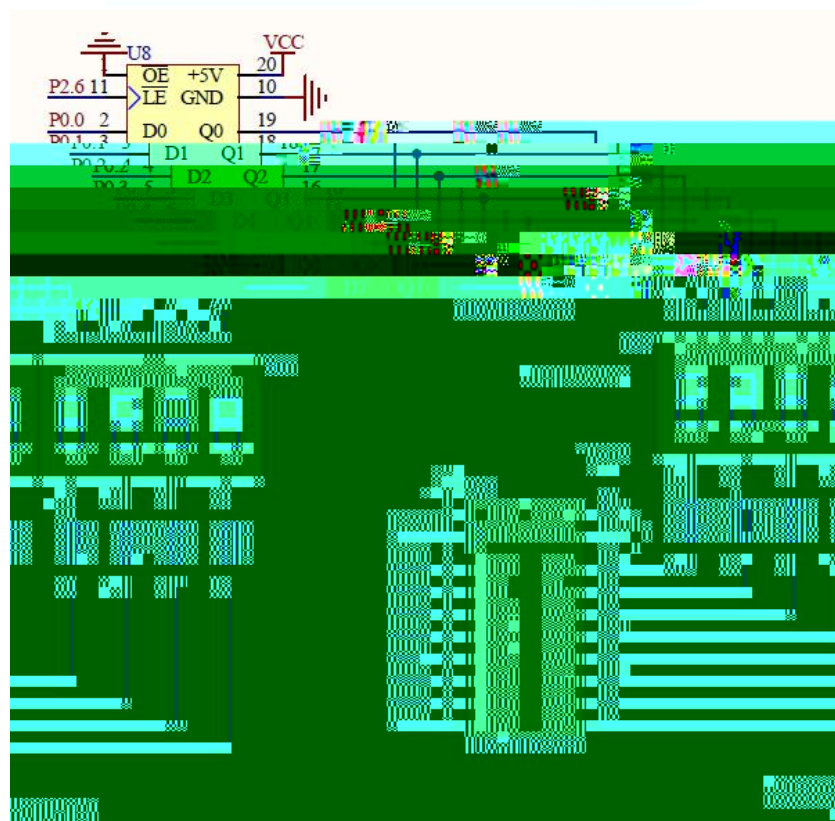
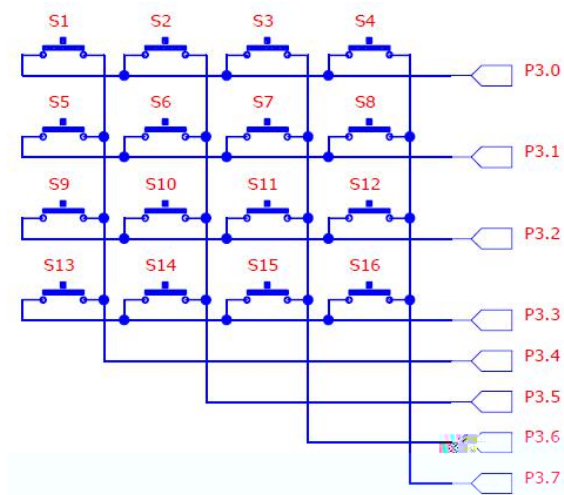
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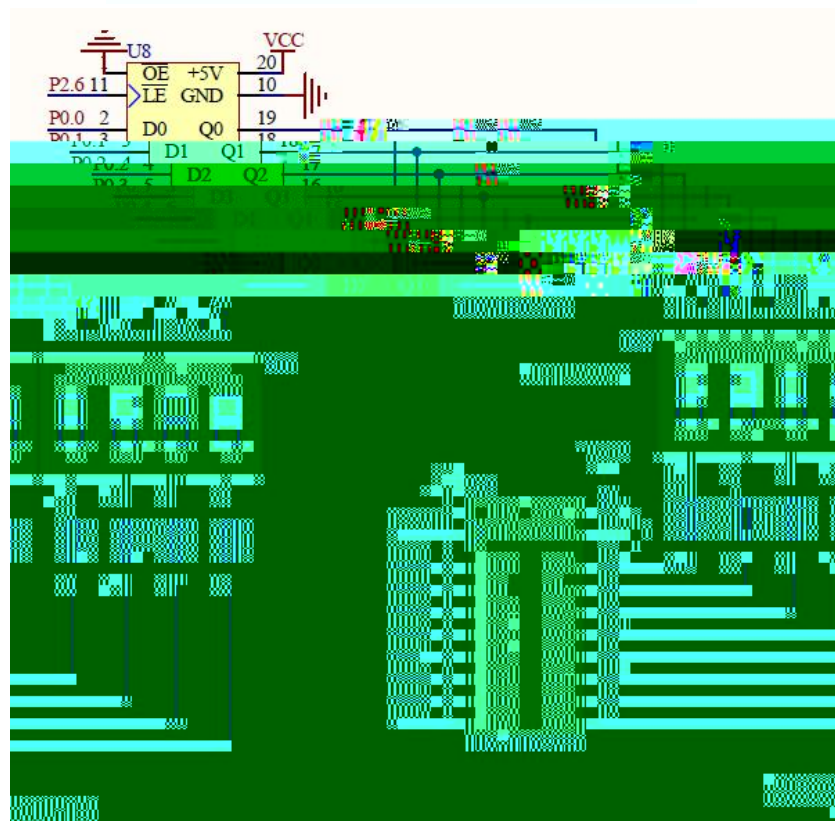
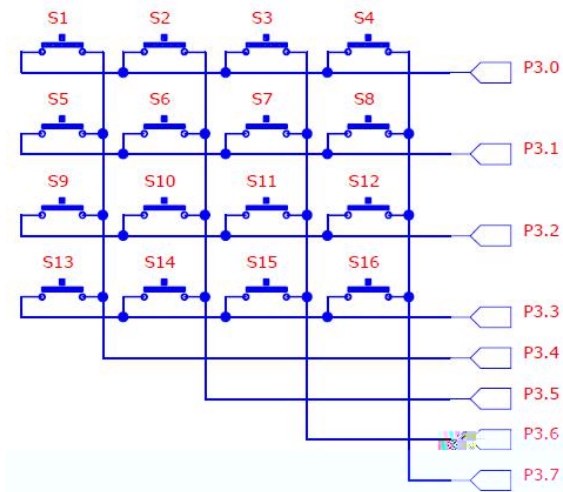
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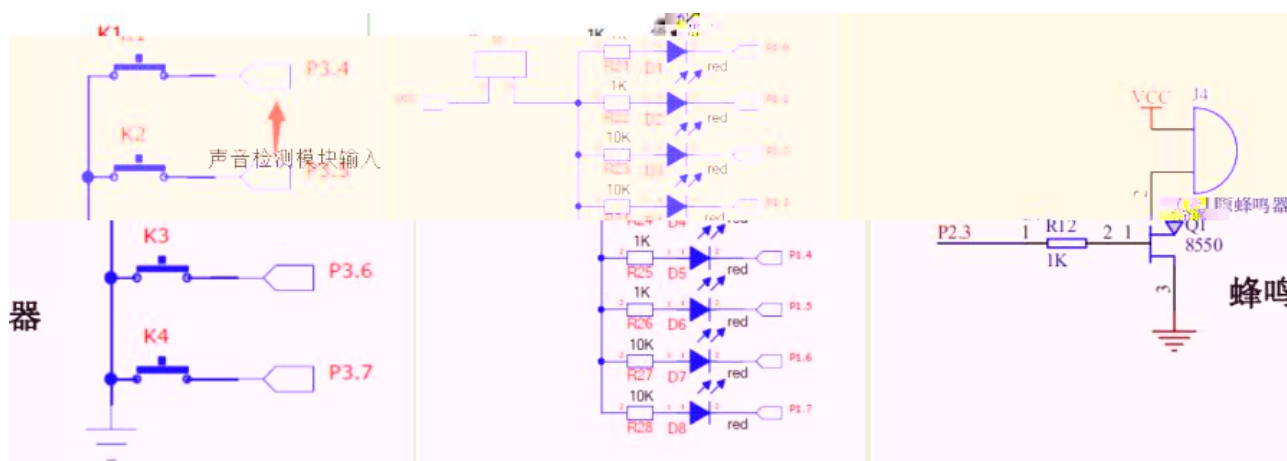
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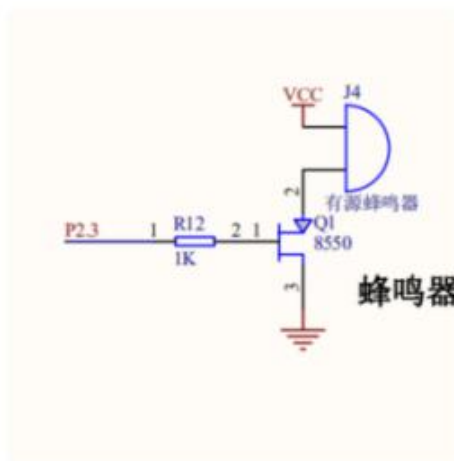
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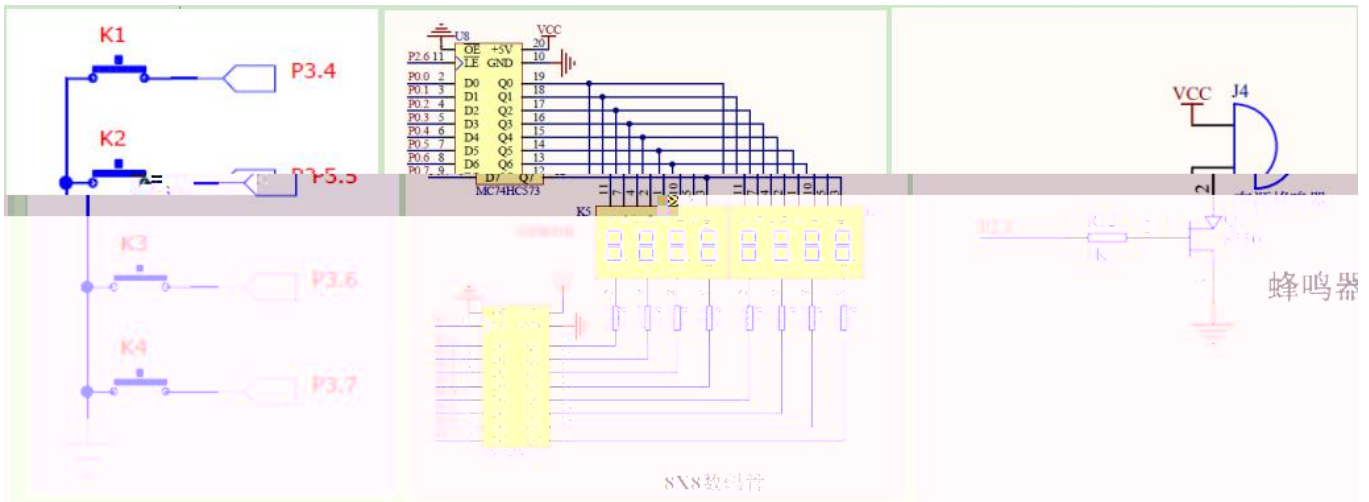
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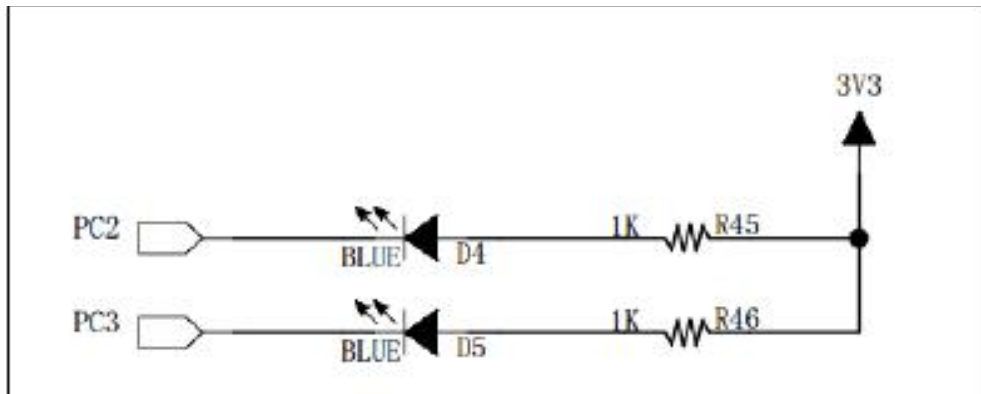
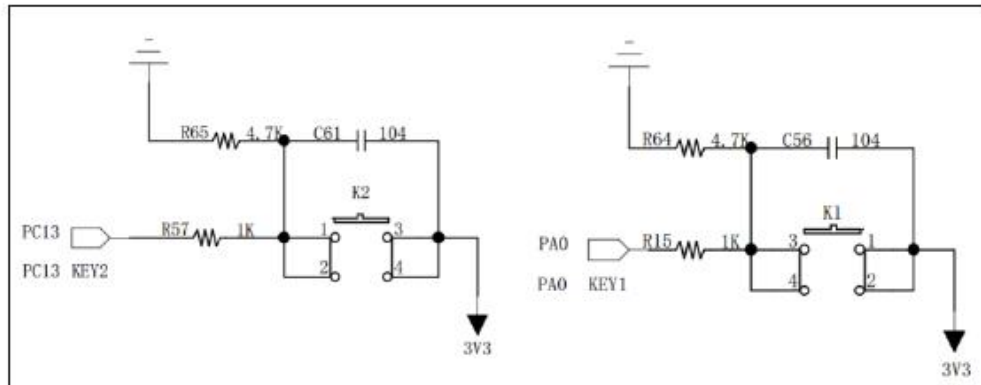
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1	VBAT	VDD	64
2	PC13/ANT1	VSS	63
3	PC14/OSC32	PB9/TIM4_CH4/SDIO_D5	62
4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN	PC12/OSCOUT	60
6	PD1/OSCOUT	PD7/I2C1_SCL/TIM4_CH2	59
7	NRES	PB6/I2C1_SCL/TIM4_CH1	58
8	PC0/ADC0	PB5/I2C1_SMBA/SPI3_MOSI/I2S3_SD	57
9	PC1/ADC1	PB4/JNTRST/SPI3_MISO	56
10	PC2/ADC2	PB3/JTDO/SPI3_SCK/I2S3_CK	55
11	PC3/ADC3	PC2/U5_RX/TIM3_ETR/SDIO_CMD	54
12	VSSA	PC12/U5_TX/SDIO_CK	53
13	VDDA	PC11/U4_RX/SDIO_D3	52
14	PA0/WKUP/ADC0/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	PC10/U4_TX/SDIO_D2	51
15	PA1/ADC1/TIM2_CH2/TIM5_CH2	PA15/JTDO/SPI3_NSS/I2S3_WS	50
16	PA2/U2_TX/ADC2/TIM2_CH3/TIM5_CH3	PA14/JTCK/SWCLK	49
17	PA3/U2_RX/ADC3/TIM2_CH4/TIM5_CH4	VDD	48
18	PC4/IO	VDD	47
19	PC5/IO	VDD	46
20	PC6/IO	VDD	45
21	PC7/IO	VDD	44
22	PC8/IO	VDD	43
23	PC9/IO	VDD	42
24	PC10/IO	VDD	41
25	PC11/IO	VDD	40
26	PC12/IO	VDD	39
27	PC13/IO	VDD	38
28	PC14/IO	VDD	37
29	PC15/IO	VDD	36
30	PD0/IO	VDD	35
31	PD1/IO	VDD	34
32	PD2/IO	VDD	33
33	PD3/IO	VDD	32
34	PD4/IO	VDD	31
35	PD5/IO	VDD	30
36	PD6/IO	VDD	29
37	PD7/IO	VDD	28
38	PD8/IO	VDD	27
39	PD9/IO	VDD	26
40	PD10/IO	VDD	25
41	PD11/IO	VDD	24
42	PD12/IO	VDD	23
43	PD13/IO	VDD	22
44	PD14/IO	VDD	21
45	PD15/IO	VDD	20
46	PD16/IO	VDD	19
47	PD17/IO	VDD	18

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1	VBAT	VDD	64
2	PC13/ANT1	VSS	63
3	PC14/OSC32	PB9/TIM4_CH4/SDIO_D5	62
4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN		
6	PD1/OSCOUT		
7	NFS		
8	PC0 ADC10		
9	PC1 ADC11		
10	PC2 ADC12		
11	PC3 ADC13		
12	VSSA		
13	VDDA		
14	PA0 WKUP ADC0-TIM2_CH1 ETR-TIM5_CH1-TIM8_ETR		
15	PA1 ADC1-TIM2_CH2-TIM5_CH2		
16	PA2 J2-TX-ADC2-TIM2_CH3-TIM5_CH3		
17	PA3 J2-RX-ADC3-TIM2_CH4-TIM5_CH4		
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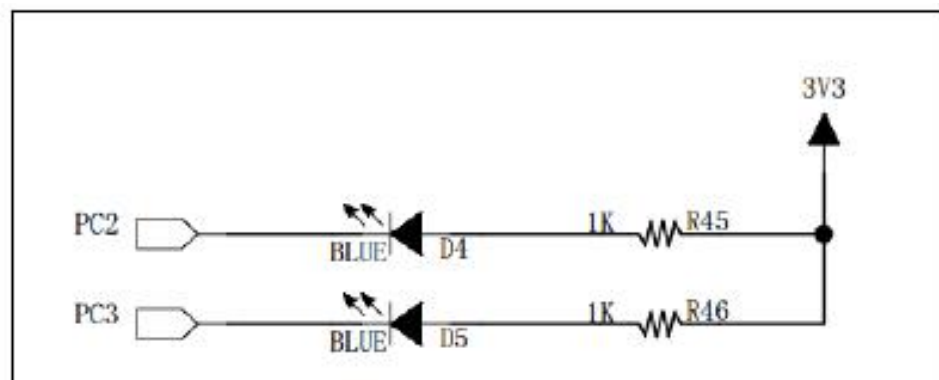
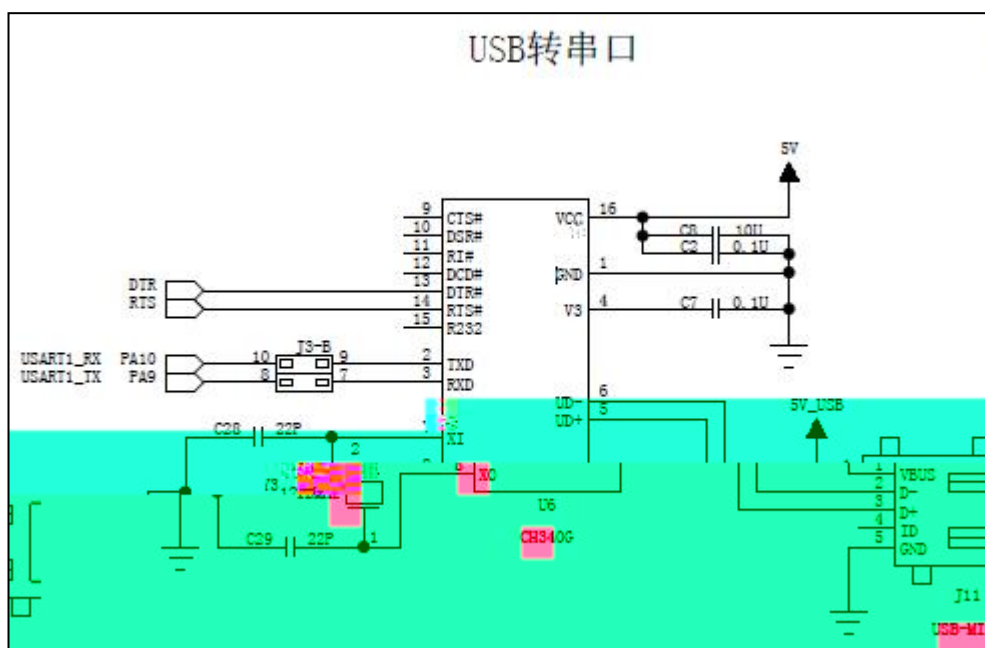




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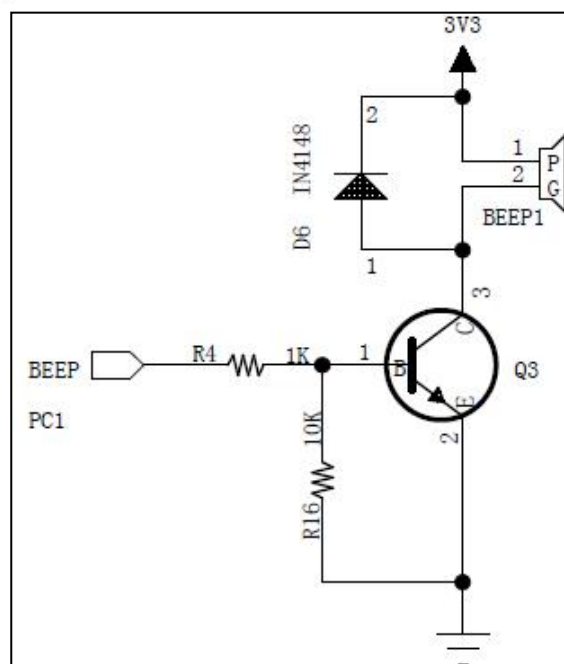
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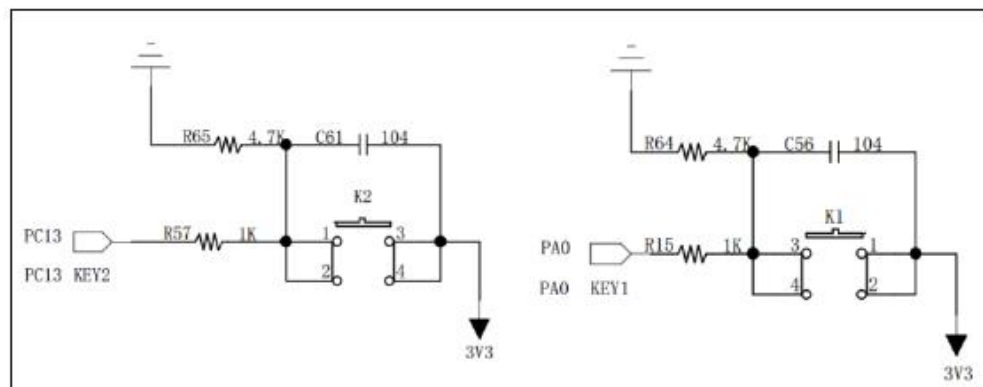
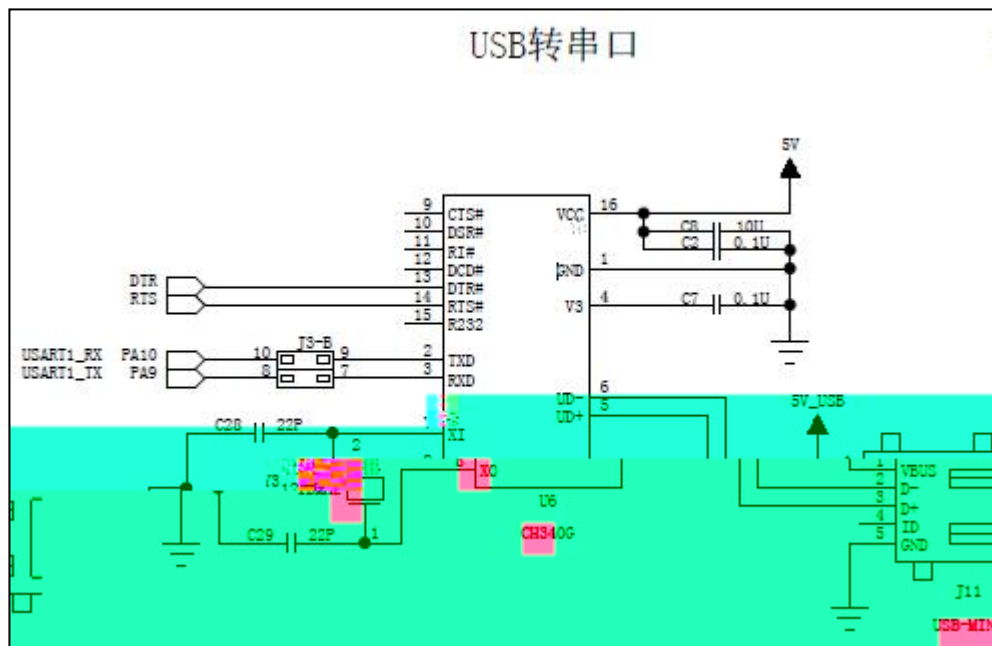


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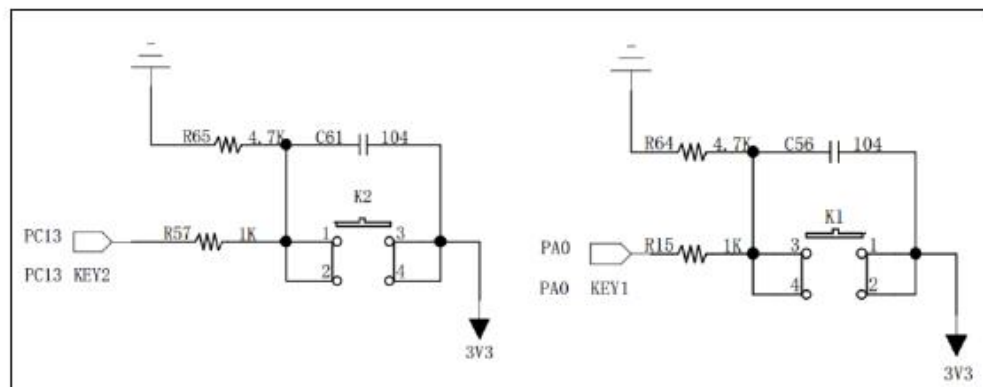
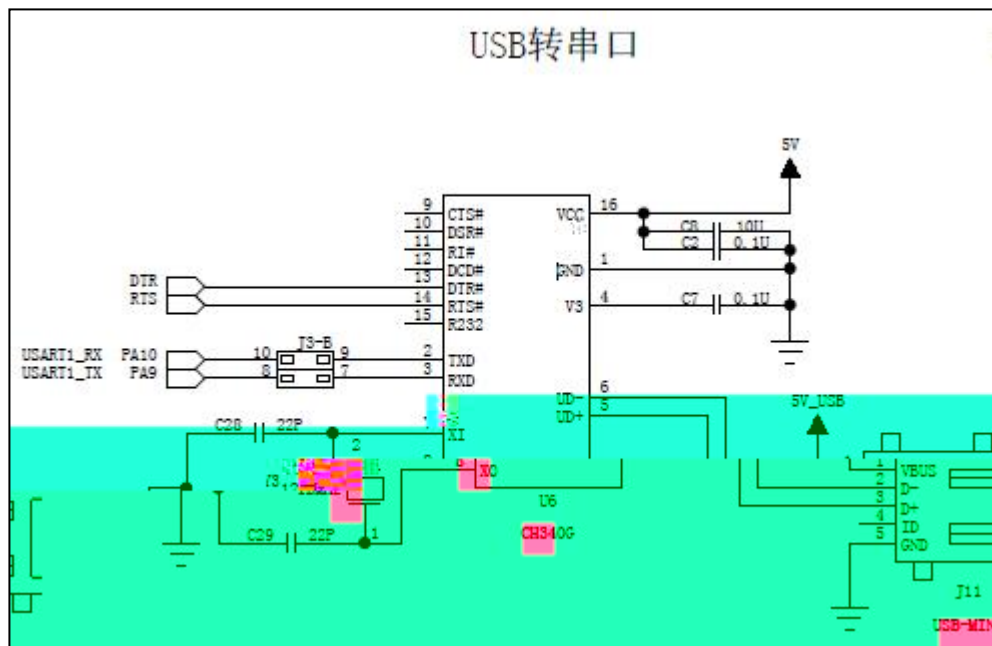


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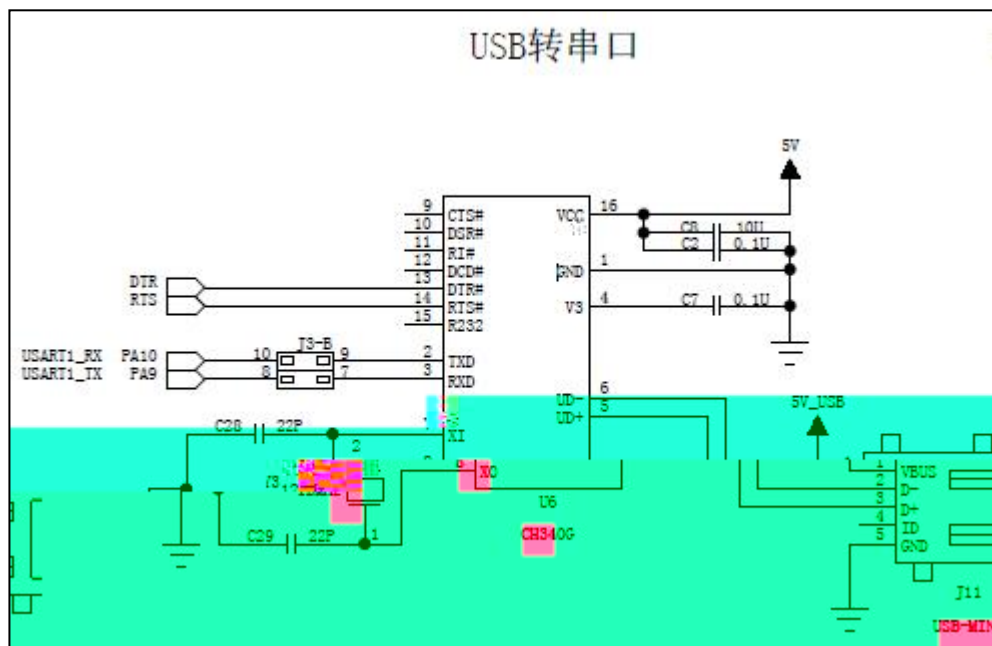
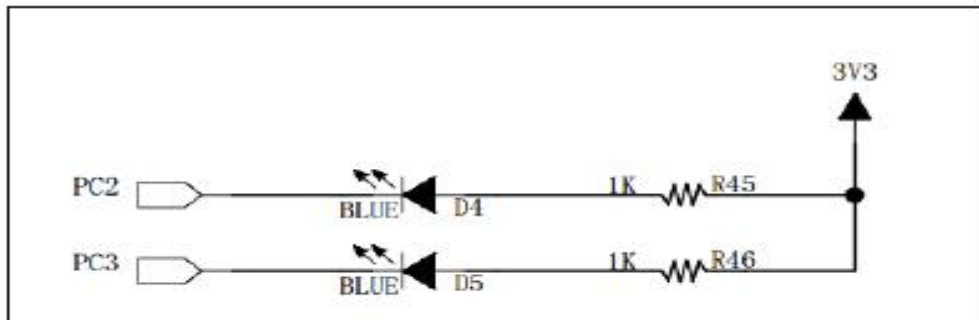


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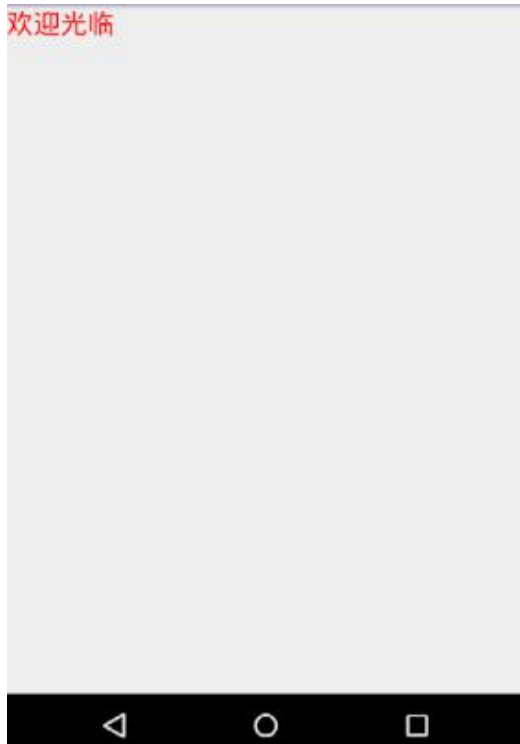
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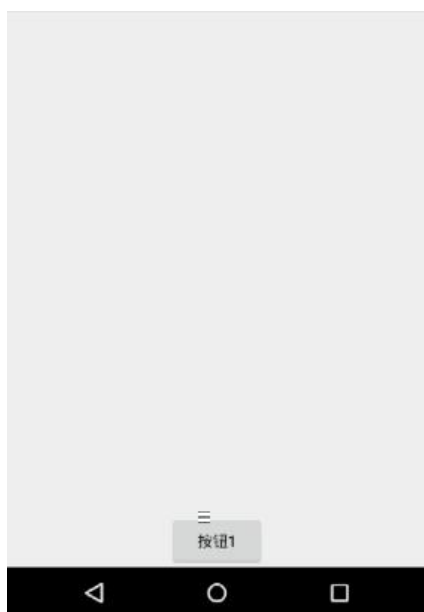
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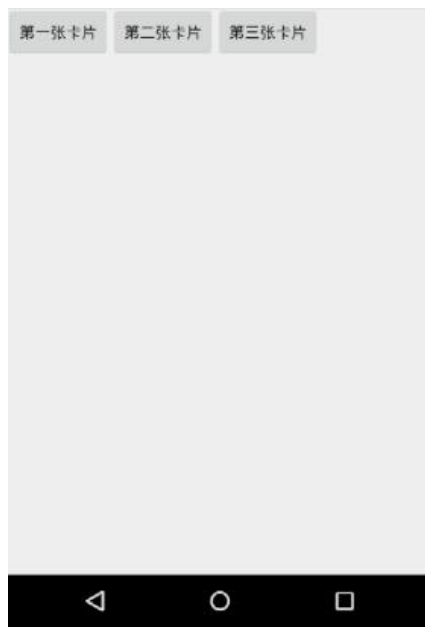
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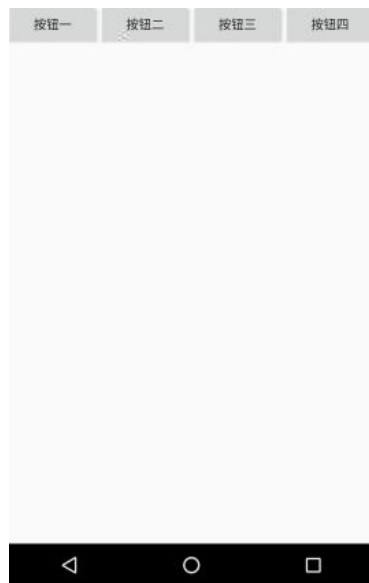
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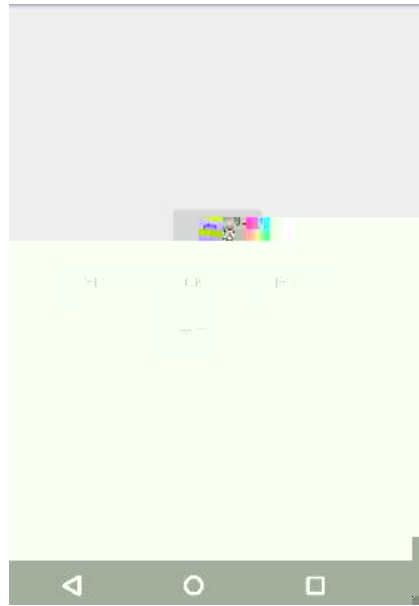


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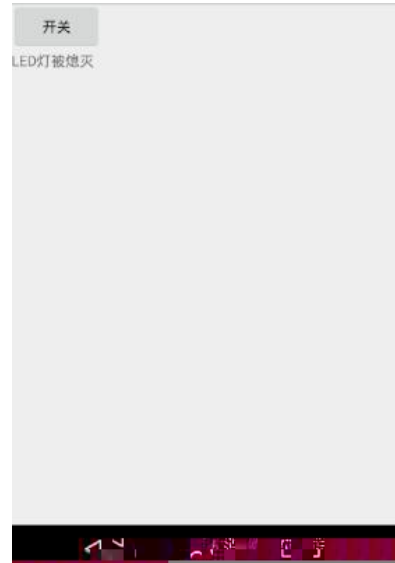
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